SHREE RAMCHANDRA EDUCATION SOCIETY'S

SHREE RAMCHANDRA COLLEGE OF ENGINEERING, LONIKAND, PUNE – 412 216

DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

LAB MANUAL

LAB PRACTICE-I

ME (VLSI AND ESD) Semester-I

INDEX

GROUP A (any three)

1. Write a program for 4*4 Matrix Keypad Interface.
2. Write a program for on-chip analog to digital conversion.
3. Write a program for I2C based seven segment LED display Interface.
4. Write a program for external interrupt.

GROUP B (any three)

1. To design, prepare layout and simulate CMOS inverter for the given specifications of load capacitance, propogation delay, power dissipation, foundry etc.
2. To design CMOs logic for F = A+B (C+D) + EFG and prepare layout. Assume suitable capacitive load and foundry. Measure TR, TF and TPD.
3. To draw FSM diagram, write VHDL code, synthesis, simulate, place and route for Tea/Coffee vending machine. Generalized I/Os of the machine are coin sense, cup sense, option sense, pour valve, timer count, alarm etc. you may assume additional I/O too.
4. To design and simulate combinational logic to demonstrate hazards. Also, simulate the same logic redesigned for removal of hazards.

GROUP C (any two)

1. To design and implement 2:1 multiplexer using transmission gate.
2. To design and implement a full adder using 4:1 multiplexer.
3. To design and implement 4 bit ALU.

GROUP D (any one)

1. Reading the data from sensor node.
2. Implement 50 stationary nodes topology using NS2 for data transmission and record QOS parameters of the network/test bed.

GROUP E (any one)

1. Design a typical research problem using scientific method.
2. Study the various analysis techniques.

Experiment No. 1

Title/Aim: Write a program for 4*4 Matrix Keypad Interface.

Objective: In this lab students will study and understand the ARM based embedded system design using Linux Operating system.

Apparatus Required:

Software:

1. Keil4.
2. Flash magic.

Hardware:

1. ARM based development board.
2. 4*4 matrix keypad.
3. RS232/USB serial cable.

Theory:

ARM 9 Architecture.
GPIO.
Keypad matrix.
LCD display.

Algorithm:

1. Start.
2. Connect Power supply to the ARM Board.
3. Connect the Board with the COM port of the PC using the serial cable.
4. Generate .hex file using Keil IDE.
5. Keep the board in ISP mode.
6. Download the .hex file.
7. Keep the board in RUN mode.
8. Press any key on on-board Keypad and you can observe the output on LCD.
9. Stop.

Conclusion:

❖ **Note:** Attach the printouts of program and its output.

Questions:

1. Why we use q_keyinit()?
2. Why we use q_lcdinit()?
3. Features of ARM9.
4. Difference between ARM7 and ARM9
5. What types of keypads are available?

Experiment No. 2

Title/Aim: Write a program for on-chip analog to digital conversion.

Objective: In this lab students will be able to do programming in embedded C for the ARM based embedded system design using Linux Operating system.

Apparatus Required:

Software:

1. Keil4.
2. Flash magic.

Hardware:

1. ARM based development board.
2. ADC.
3. RS232/USB serial cable.

Theory:

Pre-emptive and Non pre-emptive kernel.
ADC and types of ADC.

Algorithm:

1. Start.
2. Connect Power supply to the ARM Board.
3. Connect the Board with the COM port of the PC using the serial cable.
4. Generate .hex file using Keil IDE.
5. Keep the board in ISP mode.
6. Download the .hex file.
7. Keep the board in RUN mode.
8. Observe the output on LCD.
9. Stop.

Conclusion:

❖ **Note:** Attach the printouts of program and its output.

Questions:

1. Differentiate Real time OS and non real time OS.
2. What is PINSEL?
3. What do you mean by context switching.
4. When preemptive RTOS context switching occurs?
5. What is the purpose of stack in context switching?

Experiment No. 3

Title/Aim: Write a program for I2C based seven segment LED display Interface.

Objective: This program demonstrates blinking of LED using I2C.

Apparatus Required:

Software:

1. Keil4.
2. Flash magic.

Hardware:

1. ARM based development board.
2. LEDs.
3. RS232/USB serial cable.

Theory:

I2C bus.

Algorithm:

1. Start.
2. Connect Power supply to the ARM Board.
3. Connect the Board with the COM port of the PC using the serial cable.
4. Generate .hex file using Keil IDE.
5. Keep the board in ISP mode.
6. Download the .hex file.
7. Keep the board in RUN mode.
8. Observe the output on LCD.
9. Stop.

Conclusion:

- **Note:** Attach the printouts of program and its output.

Questions:

1. Where the GPIO registers are loacated and why?
2. Give the purpose of Bit Level register?
3. What is the effect of writing 1 or 0 using IOCLR instruction?
4. Write the function of FIOMASK?

Experiment No. 4

Title/Aim: To design, prepare layout and simulate CMOS inverter for the given specifications of load capacitance, propogation delay, power dissipation, foundry etc.

Objective: In this lab students will introduced to a layout based EDA tool "Micro Wind" and introduction will be accompanied with the analysis of CMOS inverter. The tool used in this Lab is Micro wind and the goals for this labs are.

1. Design of CMOS inverter using tool.
2. Prepare layout and simulate for given specification.

Apparatus Required:

Software:

1. Micro wind.

Theory:

CMOS inverter.
Characteristics of inverter.

Algorithm:

1. Start.
2. Open the Micro wind.
3. Select the foundry from file menu.
4. Select the 0.25 micron process.
5. Save the design.
6. Create CMOS inverter by using the palate.
7. Set the length and width of the device if necessary.
8. Click on generate device tab to generate the device.
9. Apply the voltages and output node using the symbol buttons from palate menu.
10. Run and simulate.
11. Analyze the simulation waveform for different voltages.
12. Increase the width and run the simulation again, analyze the effect of width on the propagation delay.
13. Similarly analyze using different widths, foundry and input voltages for load capacitance, propagation delay and power dissipation.
14. Stop.

Conclusion:

- **Note:** Attach the printouts of simulation.

Questions:

1. What is mean by backend and front end design?
2. Why Polysilicon used for gate?
3. What do you mean by technology scaling?
4. Why NMOS is preferred over PMOS?
5. What do you mean by λ parameter?

Experiment No. 5

Title/Aim: To design CMOs logic for F = A+B (C+D) + EFG and prepare layout. Assume suitable capacitive load and foundry. Measure TR, TF and TPD.

Objective: In this lab students will introduced to various CMOS logic design layout using Micro Wind. And prepare layout and simulate for given specification.

Apparatus Required:

Software:

1. Micro wind.

Theory:

CMOS fabrication and layout.
VLSI fabrication process.

Algorithm:

1. Start.
2. Open the Micro wind.
3. Select the foundry from file menu.
4. Select the 0.25 micron process.
5. Save the design.
6. Create CMOS design by using the palate.
7. Set the length and width of the device if necessary.
8. Click on generate device tab to generate the device.
9. Apply the voltages and output node using the symbol buttons from palate menu.
10. Run and simulate.
11. Analyze the simulation waveform for different voltages.
12. Increase the width and run the simulation again, analyze the effect of width on the propagation delay.
13. Add the virtual capacitance at the output.
14. Similarly analyze using different widths, foundry and input voltages for load capacitance, propagation delay and power dissipation.
15. Measure rise time and fall time.
16. Stop.

Conclusion:

- **Note:** Attach the printouts of simulation.

Questions:

1. What are the different industry standard tools used simulation and synthesis?
2. What is oxidation? Why it is necessary?
3. What is ion implantation?
4. What is mean by lithography?
5. What is metallization?

Experiment No. 6

Title/Aim: To draw FSM diagram, write VHDL code, synthesis, simulate, place and route for Tea/Coffee vending machine. Generalized I/Os of the machine are coin sense, cup sense, option sense, pour valve, timer count, alarm etc. you may assume additional I/O too.

Objective: In this lab students will introduced to digital design using VHDL. And write code, synthesis, simulate, place and route for given specification.

Apparatus Required:

Software:

1. Xilinx ISE.
2. Model-sim.

Hardware:

1. FPGA/CPLD trainer kit.
2. Interfacing cable.

Theory:

FPGA and CPLD.
VLSI design flow.
FSM and metastability.

Algorithm:

1. Start.
2. Open the Xilinx software.
3. Select the new project.
4. Select the properties in the new project wizard.
5. Select the VHDL module as source type.
6. Type the file name.
7. Write the VHDL code for Tea/Coffee vending machine.
8. Check the syntax.
9. Save the program.
10. Assign the package pins for input and output which is mentioned in entity.
11. Verify the functionality using simulator.
12. Implement design.
13. Down load the design into FPGA/CPLD board.
14. Then check the result in FPGA kit.
15. Stop.

Conclusion:

- **Note:** Attach the printouts of VHDL code and simulation.

Questions:

1. Explain elements of VHDL.
2. Explain language elements.
3. Explain modeling styles?
4. What is package?
5. Explain test bench for VHDL.

Experiment No. 7

Title/Aim: To design and implement a full adder using 4:1 multiplexer.

Objective: This lab demonstrates design and the realization of full adder circuit using multiplexer in VHDL.

Apparatus Required:

Software:

1. Xilinx ISE.
2. Model-sim.

Hardware:

1. FPGA/CPLD trainer kit.
2. Interfacing cable.

Theory:

Full adder
Multiplexer

Algorithm:

1. Start.
2. Open the Xilinx software.
3. Select the new project.
4. Select the properties in the new project wizard.
5. Select the VHDL module as source type.
6. Type the file name.
7. Write the VHDL code for adder using 4:1 multiplexer.
8. Check the syntax.
9. Save the program.
10. Assign the package pins for input and output which is mentioned in entity.
11. Verify the functionality using simulator.
12. Implement design.
13. Down load the design into FPGA/CPLD board.
14. Then check the result in FPGA kit.
15. Stop.

Conclusion:

- **Note:** Attach the printouts of VHDL code and simulation.

Questions:

1. Explain full adder and half adder?
2. Write a note on generic and configuration?
3. Differentiate function and procedure?
4. What is mean by operator overloading?
5. Define the attributes of VHDL.

Experiment No. 8

Title/Aim: To design and implement 4 bit ALU.

Objective: This lab demonstrates design of 4 bit ALU in VHDL.

Apparatus Required:

Software:

1. Xilinx ISE.
2. Model-sim.

Hardware:

1. FPGA/CPLD trainer kit.
2. Interfacing cable.

Theory:

ALU

Algorithm:

1. Start.
2. Open the Xilinx software.
3. Select the new project.
4. Select the properties in the new project wizard.
5. Select the VHDL module as source type.
6. Type the file name.
7. Write the VHDL code for 4 bit ALU.
8. Check the syntax.
9. Save the program.
10. Assign the package pins for input and output which is mentioned in entity.
11. Verify the functionality using simulator.
12. Implement design.
13. Down load the design into FPGA/CPLD board.
14. Then check the result in FPGA kit.
15. Stop.

Conclusion:

❖ **Note:** Attach the printouts of VHDL code and simulation.

Questions:

1. What is simulation?
2. What is difference between signal and variable?
3. Explain array type with example?
4. List various arithmetic operators used in VHDL.
5. Write a VHDL code for 8 bit ALU.