SHREE RAMCHANDRA EDUCATION SOCIETY'S

SHREE RAMCHANDRA COLLEGE OF ENGINEERING, LONIKAND, PUNE – 412 216

DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

LAB MANUAL

LAB PRACTICE-II

ME (VLSI AND ESD) Semester-II

INDEX

Group-A (Analog CMOS Design)-Any two

1. To design cascode current mirror for output current of 100 μA. Prepare layout and simulate. Comment on output resistance.
2. To design, prepare layout and simulate CMOS differential amplifier for CMRR of 40 dB. Comment on ICMR.
3. To design, prepare layout and simulate multistage CMOS RF amplifier in 90 nm technology for voltage gain of 60 dB, bandwidth of 100 MHz, and source impedance of 50 Ω.

Group-B (System on Chip)-Any two

1. Design, simulate and implement FSM on PLD for detection of either of input sequence X = … 1001… . or …1101… sequence and set output flags Y = "1" or Z="1" respectively. What is effect on area, speed, fan out and power by implementing this design using different state encoding styles?
2. Why gated clock is not preferred in digital design? Write Verilog code to implement CMOS layout which will generate glitch also design a RTL by Write VHDL will generate glitch and also measure it using electronic test equipment.
3. Implement temperature logging system as a co-design by Interfacing FPGA & μC 8051 as follows :
   i) LM 35 interfaced with ADC
   ii) ADC interfaced with FPGA
   iii) FPGA interfaced with μC 8051
   iv) μC 8051 is interfaced with LCD
   To display real-time room temperature. If temperature is greater than 250 C Bi-colours LED should change its normal Green color to RED color via opto-isolator by actuation of relay.

Group-C (Embedded Signal Processors)- Any two

1. Design and simulate N point FFT by targeting suitable DSP processor platform
2. Design and simulate N tap FIR filter by targeting suitable DSP processor platform.
3. Performance comparison of different filter structures.

Group-D (VLSI Interconnections)-Any two

1. Simulate RC circuit and comment on transient response.
2. Simulate startup model of RLC.
3. Simulate a transmission line and evaluate VSWR, Reflection coefficient parameters considering different loading considerations using analog simulation tool.

Experiment No. 1

Title/Aim: To design cascode current mirror for output current of 100 µA. Prepare layout and simulate. Comment on output resistance.

Objective: The objective of this assignment is analysis, modeling, simulation, and design of analog circuits implemented in CMOS technology for given specifications.

Apparatus Required:

Software:

1. Microwind/Ni2/Mentor graphics.

Theory:

1. Active and passive current mirror circuits.
2. Types of current mirror circuit.

Algorithm:

1. Start.
2. Open the Micro wind.
3. Select the foundry from file menu.
4. Save the design.
5. Design CMOS current mirror for 100 µA by using the palate.
6. Set the length and width of the device if necessary.
7. Click on generate device tab to generate the device.
8. Apply the voltages and output node using the symbol buttons from palate menu.
9. Run and simulate.
10. Analyze the simulation waveform for different output resistances.
11. Increase the width and run the simulation again, analyze the effect of width on the output response.
12. Similarly analyze using different widths, foundry and input voltages for resistances.
13. Stop.

Conclusion:

❖ **Note:** Attach the printouts of design and simulation.

Questions:

1. Why CMOS is preferred for mixed signal design?

2. What is current mirror/amplifier?

Experiment No. 2

Title/Aim: To design, prepare layout and simulate CMOS differential amplifier for CMRR of 40 dB. Comment on ICMR.

Objective: In this lab students will be able learn and design of differential amplifier for given specifications.

Apparatus Required:

Software:

1. Microwind/Ni2/Mentor graphics.

Theory:

1. P-channel differential amplifier.
2. N-channel differential amplifier.

Algorithm:

1. Start.
2. Open the Micro wind.
3. Select the foundry from file menu.
4. Save the design.
5. Design CMOS differential amplifier for 40 dB using the palate.
6. Set the length and width of the device if necessary.
7. Click on generate device tab to generate the device.
8. Apply the voltages and output node using the symbol buttons from palate menu.
9. Run and simulate.
10. Stop.

Conclusion:

❖ **Note:** Attach the printouts of design and simulation.

Questions:

1. What are the features of differential amplifier?

2. What is CMIR?

Experiment No. 3

Title/Aim: Design, simulate and implement FSM on PLD for detection of either of input sequence X = … 1001... . or …1101… sequence and set output flags Y = "1" or Z="1" respectively. What is effect on area, speed, fan out and power by implementing this design using different state encoding styles?

Objective: The objective of this assignment design of FSM using different encoding techniques.

Apparatus Required:

Software:

1. Xilinx ISE.
2. Model-sim.

Hardware:

1. FPGA/CPLD trainer kit.
2. Interfacing cable.

Theory:

1. FSM
2. State encoding techniques.

Algorithm:

1. Start.
2. Open the Xilinx software.
3. Select the new project.
4. Select the properties in the new project wizard.
5. Select the VHDL module as source type.
6. Type the file name.
7. Write the VHDL code for sequence detector.
8. Check the syntax.
9. Save the program.
10. Assign the package pins for input and output which is mentioned in entity.
11. Verify the functionality and simulate for area, speed and fan out.
12. Implement design.
13. Down load the design into FPGA/CPLD board.
14. Then check the result in FPGA/CPLD kit.
15. Repeat the step from 7 to 14 for different encoding style.
16. Stop.

Conclusion:

- **Note:** Attach the printouts of VHDL program and its output.

Questions:

1. What are the advantages and disadvantages of FSM?
2. What is sequential circuit?
3. What is advantage of state reduction technique?

Experiment No. 4

Title/Aim: Implement temperature logging system as a co-design by Interfacing FPGA & µC 8051 as follows :

i) LM 35 interfaced with ADC

ii) ADC interfaced with FPGA

iii) FPGA interfaced with µC 8051

iv) µC 8051 is interfaced with LCD

To display real-time room temperature. If temperature is greater than 250 C Bi-colours LED should change its normal Green color to RED color via Opto-isolator by actuation of relay.

Objective: In this lab students will understand the co-design of FPGA and microcontroller for given application.

Apparatus Required:

Software:

1. Xilinx ISE.
2. Model-sim.
3. Keil4.

Hardware:

1. FPGA/CPLD trainer kit.
2. Microcontroller board.
3. LM 35 sensor.
4. ADC module.
5. LCD module.
6. Interfacing cable.

Theory:

1. FPGA architecture.
2. 8051 architecture.

Algorithm:

1. Start.
2. Interface the ADC module with FPGA board.
3. Write the VHDL code in Xilinx to read the real time room temperature.
4. Download the code in FPGA board.
5. Display the output using bi color LEDs on FPGA board.
6. Now connect the 8051 controller to FPGA board and LCD module.
7. Write the code for 8051 in Keil to read and display the real time data serially from FPGA

board.

8. Download the hex file in 8051.
9. LCD module will display the real time temperature.
10. Stop.

Conclusion:

❖ **Note:** Attach the printouts of programs.

Questions:

1. What are the voltage and current specifications of FPGA I/O pins?
2. What are the voltage and current specification of microcontroller I/O pins?
3. Explain SoC technology.
4. Enlist the real time applications of SoC.

Experiment No. 5

Title/Aim: Design and simulate N point FFT by targeting suitable DSP processor platform

Objective: In this lab students will understand the signal processing application in embedded system.

Apparatus Required:

Software:

1.

Hardware:

DSP trainer kit.

Theory:

1. DFT
2. FFT

Algorithm:

1. Start.
2. Write code for FFT algorithm.
3. Download the code into DSP processor.
4. Repeat the procedure for various values of N.
5. Stop.

Conclusion:

- **Note:** Attach the printouts if necessary.

Questions:

1. What is FFT? Why FFT is needed.
2. How many multiplication and addition are required to compute N-point DFT using radix-2FFT.
3. What is decimation-in-time domain algorithm?

4. What is decimation-in-frequency domain algorithm?
5. What is the basic operation of DIT algorithm?

Experiment No. 6

Title/Aim: Design and simulate N tap FIR filter by targeting suitable DSP processor platform.

Objective: The objective of this assignment is to understand the frequency selective circuits for signal processing application in embedded system design.

Apparatus Required:

Software:

Hardware:

DSP trainer kit.

Theory:

FIR filters.

Algorithm:

1. Start.
2. Write code for FIR filter algorithm.
3. Download the code into DSP processor.
4. Stop.

Conclusion:

❖ **Note:** Attach the printouts if necessary.

Questions:

1. What are the disadvantages of Fourier series method?
2. What is Gibbs phenomenon?
3. What are the desirable characteristics of the window?
4. What is window and why it is necessary?
5. For what type of filters frequency sampling method is suitable?

Experiment No. 7

Title/Aim: Simulate RC circuit and comment on transient response.

Objective: Objective of the assignment is to learn and design RC network in VLSI interconnects.

Apparatus Required:

Software:

1. Multisim/Proteus/Mentor graphics/Matlab.

Theory:

RC network in VLSI.

Algorithm:

1. Start.
2. Design and simulate in any software mentioned above.
3. Change the parameters of each component and simulate.
4. Stop.

Conclusion:

- **Note:** Attach the printouts of simulation.

Questions:

1. Explain passive RC network?
2. What are the characteristics of RC network?

Experiment No. 8

Title/Aim: Simulate start up model of RLC.

Objective: Objective of the assignment is to learn and design RLC network in VLSI interconnects.

Apparatus Required:

Software:

1. Multisim/Proteus/Mentor graphics/Matlab.

Theory:

RLC network in VLSI.

Algorithm:

1. Start.
2. Design and simulate in any software mentioned above.
3. Change the parameters of each component and simulate.
4. Stop.

Conclusion:

- **Note:** Attach the printouts of simulation.

Questions:

1. Explain passive RLC network?
2. What are the characteristics of RLC network?